Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of fabricating a capacitor comprising:
generating a first layer of silicon nitride upon a silicon substrate;
depositing a high dielectric constant material layer;
generating a second layer of silicon nitride by applying an ultra-high vacuum and depositing silicon nitride; and
generating an electrode layer upon the second layer.

[c2] The method of claim 1, further comprising the step of cleaning the silicon substrate using hydroflouric acid (HF) prior to generating the first layer.

[c3] The method of claim 1, wherein the step of generating the first layer includes conducting a rapid thermal nitridation in ammonia (NH_3).

[c4] The method of claim 1, wherein the first layer is no less than approximately 5Åand no greater than approximately 15Å.

[c5] The method of claim 1, wherein the high dielectric constant material is chosen from the group consisting of: aluminum oxide, hafnium oxide (HfO_2), zirconium oxide (ZrO_2), lanthanum oxide (LaO_2), silicates of the preced-

ing, strontium titanate (STO), tantalum oxide (Ta_2O_5), a mixture dielectric of hafnium oxide (HfO_2) and aluminum oxide (Al_2O_3)($HfAlO_x$) and a mixture dielectric of zirconium oxide (ZrO_2) and aluminum oxide (Al_2O_3)($ZrAlO_x$).

[c6] The method of claim 1, wherein the high dielectric constant material layer is no less than approximately 15Å thick and no greater than approximately 50Å thick.

[c7] The method of claim 1, wherein the step of generating the second layer includes cleaning the high dielectric constant material layer in situ prior to depositing the second layer.

[c8] The method of claim 1, wherein the high dielectric constant material layer has a surface temperature of no less than approximately 600°C and no greater than approximately 900°C during the step of generating the second layer.

[c9] The method of claim 1, wherein the ultra-high vacuum is at no less than approximately 10^{-6} Torr and no greater than approximately 10^{-2} Torr.

[c10] The method of claim 1, wherein the step of depositing the second layer includes chemical vapor deposition (CVD) using silane (SiH_4) and ammonia (NH_3) as silicon (Si) and nitrogen (N) precursors.

[c11] The method of claim 1, wherein the second layer is no less than approximately 3Å thick and no greater than approximately 8Å thick.

[c12] The method of claim 1, further comprising the step of conducting a thermal anneal.

[c13] A method of fabricating a capacitor, the method comprising the steps of:
conducting a rapid thermal nitridation in ammonia (NH_3) to generate a first layer of silicon nitride upon a silicon substrate;
depositing a layer including an aluminum oxide;
applying an ultra-high vacuum;
chemical vapor depositing (CVD) silicon nitride in the ultra-high vacuum; and
generating an electrode layer upon the second layer.

[c14] The method of claim 13, further comprising the step of cleaning the silicon substrate in hydrofluoric acid (HF) prior to generating the first layer.

[c15] The method of claim 13, wherein the step of generating the second layer includes cleaning the aluminum oxide in situ prior to the CVD of the second layer.

[c16] The method of claim 15, wherein the aluminum oxide

has a surface temperature of no less than approximately 600°C and no greater than approximately 900°C during the step of generating the second layer.

[c17] The method of claim 13, wherein the ultra-high vacuum is at no less than approximately 10^{-11} Torr and no greater than approximately 10^{-8} Torr when idle and no less than approximately 10^{-6} Torr and no greater than approximately 10^{-2} Torr during silicon nitride deposition.

[c18] The method of claim 13, wherein the step of CVD uses silane (SiH_4) and ammonia (NH_3) as silicon (Si) and nitrogen (N) precursors.

[c19] The method of claim 13, further comprising the step of conducting a thermal anneal.

[c20] A capacitor comprising:
a silicon substrate;
a first layer of silicon nitride upon the silicon substrate;
a high dielectric constant layer upon the first layer;
a second layer of silicon nitride having monolayer quantities of the silicon nitride;
and
an electrode layer upon the second layer.